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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,841	07/31/2003	Chun Shiah	ET01-010	1036
7590 06/23/2004			EXAMINER	
STEPHEN B. ACKERMAN 28 DAVIS AVENUE POUGHKEEPSIE, NY 12603			NGUYEN, LONG T	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 06/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/631,841

Applicant(s)

SHIAH, CHUN

Examiner

Long Nguyen

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 10/29/03.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

On page 4, line 12-13, the recitation “a signal VB1 is applied to the gate nodes of P1 and P2” is objected to because VB1 is not a signal. In fact, VB1 is just a bias voltage node for P1 and P2, and this bias voltage node VB1 is formed by the connection of the drain of P1 to the gates of P1 and P2. Appropriate correction and/or clarification to the above phrase is required.

Similarly, on page 5, line 7-8, the recitation “a signal VB11 is applied to the gate nodes of P11 and P12” is objected to because VB11 is not a signal. In fact, VB1 is just a bias voltage node for P1 and P2. Appropriate correction and/or clarification to the above phrase is required.

Claim Objections

2. Claims 2 and 11 are objected to because of the following informalities:

In claim 2, line 2, “an” should be changed to --the--.

In claim 2, line 3, “a VSS” should be changed to --the VSS--.

In claim 2, line 5, it appears that “a signal VB11 is applied” should be changed to --the PMOS bias node is formed-- for similar reason as discussed in the objection to the specification and to prevent of indefinite problem.

In claim 2, lines 7-8 and 10, it appears that “a signal VB11 is applied” should be changed to --the bias PMOS bias node is formed--.

In claim 2, line 11, “an” should be changed to --the--.

In claim 2, line 13, “a VSS” should be changed to --the VSS--.

In claim 2, line 14, “an” should be changed to --the--.

In claim 11, line 2, "a SIGNAL_OUT1." should be changed to --the output signal SIGNAL_OUT1.--

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, "a large capacitance" is indefinite because it is not know if it refers to a capacitance value or a capacitance element. Further, "large" is a relative term and it is not clear at what value is considered to be "larger". Further, "a PMOS bias node" is indefinite because it is not clear whether the PMOS bias node is of the buffer input portion or whether it is outside of the buffer input portion. Further, the claim is indefinite because there is no connection between the elements in the claim.

Claims 2-11 are indefinite because they include the indefiniteness of claim 1.

In claims 3-9, the transistors recited in these claims lack antecedent basis. It appears that these claims 3-9 should depend on claim 2 rather than claim 1.

In claims 10 and 11, the recitation "a large capacitance coupling ratio" is indefinite because it is not known a ratio of what. Further "large capacitance" is indefinite as discussed in claim 1 above.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Shim et al. (UPS 6,437,613).

With respect to claims 1-11, Figure 6 of the Shim et al. reference discloses a circuit, which includes: a buffer input portion (all elements in 61 except for 61a) receiving an input signal (VPUMPL); a capacitance element (61a); a PMOS bias node (the node connected the gates of the PMOS transistors together); and a buffer output portion (65) for providing an output signal (JCLK). Note that, the transistors read in Figure 6 the claims are the first transistor (the NMOS transistor having gate receiving VPUMPL), the second transistor (the PMOS transistor having gate and drain connected together), the third transistor (the PMOS transistor having its drain VCOML connected to 65), and the fourth transistor (the NMOS transistor having its gate receiving VREF). Note that, for claim 8, the buffer output portion (65) comprises a first inverter because when VCOMR is Hi, the JCLK is the inverted of VCOML. For claims 9-11, because the structure of the claims is fully met so the functional limitations of these claims are deemed to be met.

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Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 22, 2004



Long Nguyen
Primary Examiner
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